s_thyristor_bridge_3ph_2 (subcircuit)

Attributes

```
inputs: g1
outputs:
e_left_nodes: a b c
e_right_nodes: p m
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes:
b_top_nodes:
b_bottom_nodes:
parameters:
  cap: 10p
  flag_frequency: 1
  flag_period: 0
  frequency: 50
  r_off: 10M
  r_on: 1m
  T: 20m
  v_on: 0
  x_high: 1
```

Description

s_thyristor_bridge_3ph_2 is the 3-phase thyristor bridge circuit shown in the figure. The gate signal g1 is externally supplied, and the other gate signals are internally derived from g1 by setting n_delay of the edge_delay elements to 1, 2, 3, 4, or 5 (see the documentation of edge_delay.xbe). The theta_delay parameter for all of the edge_delay elements is set to 60, resulting in a phase shift of 60°, 120°, 180°, 240°, 300° with respect to g1.

The thyristor parameters are specified by r_on, r_off, v_on, x_high (see the documentation for thyristor.ebe). cap specifies each of the three capacitances shown in the figure.

The parameters flag_frequency, flag_period, frequency, T, x_high are passed on to the edge_delay elements.

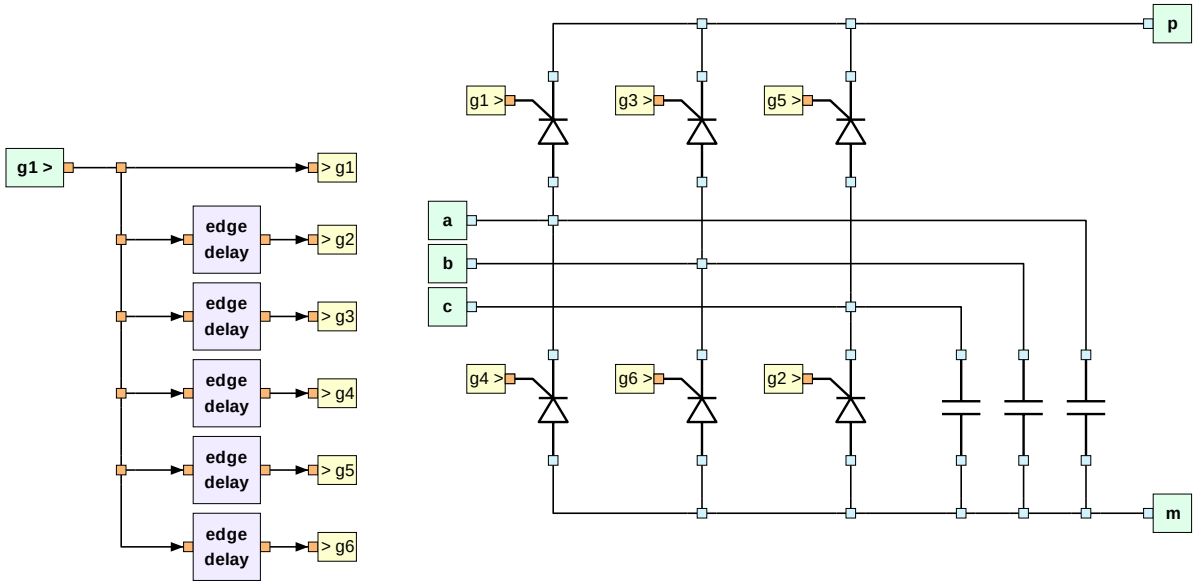

Figure 1: Schematic diagram of `s_thyristor_bridge_3ph_2`.