s_clock_4 (subcircuit)

Attributes

```
inputs:
outputs: y1 y2 y3 y4
e_left_nodes:
e_right_nodes:
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes:
b_top_nodes:
b_bottom_nodes:
parameters:
  T: 20m
  alpha: 10
  beta: 0
  delta1: 0.01m
  delta2: 0.01m
  y_high: 1
```

Description

s_clock_4 generates four gate signals (outputs y1, y2, y3, y4), varying between 0 and y_high. It uses four clock_3.xbe blocks with indx values varying from 1 to 4. The variation of y1, y2, y3, y4 with time is described in the documentation for clock_3.xbe.