

s_gate_pulses_1ph_2 (subcircuit)

Attributes

```
inputs: x1 x2
outputs: y1 y2
e_left_nodes:
e_right_nodes:
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes:
b_top_nodes:
b_bottom_nodes:
parameters:
  delt_min: 1e-6
  delt_nrml: 10e-6
  t_delay: 1e-3
  y_high: 1
```

Description

s_gate_pulses_1ph_2 generates signals required to drive a pair of switches in a “non-overlapping” manner. It compares inputs x_1 and x_2 and produces outputs y_1 and y_2 . The value of y_1 is y_{high} if $x_1 > x_2$; else, it is zero. For y_2 , the opposite is true; viz., y_2 is equal to y_{high} if $x_1 < x_2$; else, it is zero. However, a delay given by the parameter t_{delay} is introduced between the transitions in y_1 and y_2 . (See the documentation for s_gate_pulses_1ph_1.)

The parameters $delt_{min}$, $delt_{nrml}$ are used for controlling the simulator time steps (see documentation for cmpr_1_1).

In terms of functionality, s_gate_pulses_1ph_2 is similar to s_gate_pulses_1ph_1; however, s_gate_pulses_1ph_2 involves fewer elements and is therefore more efficient.