s_clock_3ph_6 (subcircuit)

Attributes

```
inputs:
outputs: y1 y2 y3 y4 y5 y6
e_left_nodes:
e_right_nodes:
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes:
b_top_nodes:
b_bottom_nodes:
parameters:
  D: 0.5
  T: 1m
  alpha: 0
  dt: 0.01m
  flag_frequency: 1
  flag_period: 0
  frequency: 1k
```

Description

s_clock_3ph_6 generates six gate signals (outputs y1, y2, y3, y4, y5, y6), varying between 0 and 1, for 3-phase applications. It uses six clock_3ph.xbe blocks with index1 values varying from 1 to 6, thus giving a phase shift of 60° between consecutive outputs.

Its parameters flag_frequency, flag_period, frequency, T, D, alpha, dt have the same meaning as the corresponding parameters of clock_3ph.xbe.

The outputs y1, y2, y3, y4, y5, y6 are made available as output variables.