s_thyristor_bridge_1ph (subcircuit)

Attributes

```
inputs:
outputs:
e_left_nodes: a b
e_right_nodes: p m
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes:
b_top_nodes:
b_bottom_nodes:
parameters:
  T: 20m
  alpha: 0
  cap: 10p
  dt: 0.1u
  flag_frequency: 1
  flag_period: 0
  frequency: 50
  r_off: 10M
  r_on: 1m
  tw_deg: 10
  v_on: 0
  x_high: 1
```

Description

s_thyristor_bridge_1ph is the thyristor bridge circuit shown in the figure where the thyristor clock pulses are internally generated by s_clock_thyr_2.

The thyristor parameters are specified by r_on, r_off, v_on, x_high (see the documentation for thyristor.ebe). cap specifies the capacitances connected between a and m and between b and m.

The parameters flag_frequency, flag_period, frequency, T, alpha, dt, tw_deg, x_high are passed on to the two clock_thyr elements within s_clock_thyr_2. The beta values assigned to the two clock_thyr elements are 0 and 180 (see the documentation for clock_thyr.ebe for sample waveforms).

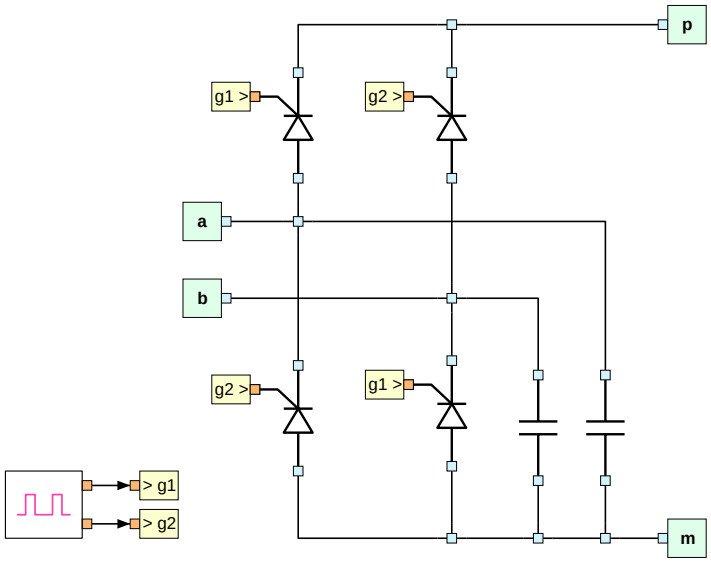

Figure 1: Schematic diagram of `s_thyristor_bridge_1ph`.