s_clock_thyr_2 (subcircuit)

Attributes

```
inputs:
outputs: y1 y2
e_left_nodes:
e_right_nodes:
e_top_nodes:
e_bottom_nodes:
b_left_nodes:
b_right_nodes:
b_top_nodes:
b_bottom_nodes:
parameters:
  T: 1
  alpha: 0
  dt: 1u
  flag_frequency: 1
  flag_period: 0
  frequency: 1
  tw_deg: 0
  x_high: 1
```

Description

s_clock_thyr_2 generates two gate signals (outputs y1, y2), varying between 0 and x_high, typically used in thyristor circuits. It uses two clock_thyr.xbe blocks with beta equal to 0 or 180. The variation of y1 and y2 with time is described in the documentation for clock_thyr.xbe.